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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,196	09/15/2003	Kuo-Jung Tung	CNTP0007USA	2195

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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EXAMINER	
NGUYEN, NHA T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,196	TUNG ET AL.	
	Examiner	Art Unit	
	Nha Nguyen	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

The description of the disclosure needed to be indented and formatted to help with clarification of the disclosure. There were a lot of typos in the specification, where words are connected together and needed space out. This can be seen in paragraph [0005] with "generatedwhile", paragraph [0012] with "30indicates" – "untilthe", paragraph [0030] with "orone", paragraph [0031] with "conditionsbranch". In paragraph [0031], remove "on" from "on only a single condition branch". In paragraph [0030], "in order to transmit the result of executing the user program 40 until the address back to the host computer 34" – is not very clear. This statement was interpreted as " in order to transmit the result of the executing of the user program 40 back to the host computer" for examination purposes.

See MPEP 608.01

Appropriate correction is required.

Claims Objection

Claim 1 is objected to because of misspelling. The term "Proving" in claim 1 line 6, should be replaced by providing.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims **1-6, and 8-11** are rejected under 35 U.S.C. 102(e) as being anticipated by **Ok** et al, (US Patent No.6,934,886) hereinafter **Ok**.

As per Claim 1, Ok discloses a microprocessor system capable of software debug (See Ok, Figure 2 and also Col 3; lines 23-25) comprising:

a host computer for executing remote debug (See Ok, Figure 2, "10 – Host Computer" and also see Abstract; lines 1-6).

a program memory for storing a monitor program for providing monitoring of the host computer and a user program (See Figure 2, "Debugger Controller" , "Status Signal – providing information back to host"). "Debugger Controller" mention in reference act as a monitor of the host computer and a user program because the debugger controller feed back the status of the debugging process back to the host, is there forth doing a monitor task. (See Col 3; lines 44-47).

at least one break point address holder for temporarily storing a break point address from the host computer (See Figure 5; "S11" and also see Col 4; Lines 53-54);

a break point comparator unit connected to the break point address holder for comparing the break point address from the break point address holder with an address of the user program being executed (See Figure 3; "53 – Address Comparator" and also see Col 3/4; Lines 66-67:1-4),

and for outputting an interrupt control signal when the addresses match (See Abstract; Lines 8-13 and also See figure 5; "S20- ***Output Break Signal***");

a controller for controlling the break point comparator unit (See Col 2; Lines 32-40, "***Memory Break Controller***"). Where "***Memory Break Controller***" is the "**controller for the breakpoint comparator unit**" mentioned in the claim because they both perform the same function of controlling the comparator and identifying address accessed and address observed.

and a microprocessor electrically connected to the host computer comprising: (See Figure 2). Figure 2 showed connection between the Host computer and the microprocessor to send signals.

a host interface connected to a transmit port of the host computer for transmitting signals between the microprocessor and the host computer (See Figure 2, "Control Signal, Status Signal, Data Signal", and Also See Col 2; Lines 24-40, "Performing a debugging process on the processor upon ***receipt of command from a host computer***.....***transmitting*** the address and corresponding information data ***to the host computer*** through the debugger controller". Reference discloses sending and receiving of data between the host and the microprocessor, it is inherent that the host have an interface which allow it to connect to the microprocessor for transmitting and receiving of data.

a program memory address pointer for indicating an address of the program memory (See Col 3; Lines 36-37, "break point sensing unit for ***observing an address of the program memory*** accessed by the processor"). It is inherent that the reference disclosures use a pointer to locate the current address in memory because break point sensing unit is observing current address access by the processor.

and outputting the address of the user program being executed to the break point comparator unit (See Col 3; Lines 37-42). Ok showed that current address is being compare to break point address, which is the user program address from the memory address pointer;

and an interrupt control unit for receiving the interrupt control signal from the break point comparator unit (See Col 6, Lines 30-37, "memory break control register outputs a break signal to the processor in order to discontinue program operation", Also see See Fig 2, "***Breakpoint sensing unit***" – Also See Col 3; lines 36-41). The "***breakpoint sensing unit***" is the unit for receiving interrupt control signal from the break point comparator unit.

wherein when the interrupt control unit receives the interrupt control signal from the break point comparator unit (See Fig 2, "***Breakpoint sensing unit***" – Also See Col 3; lines 36-41), the microprocessor executes the monitor program in the program memory in order to transmit the status of execution of the user program to the host computer (See Col 2; Lines 38-40, "***transmitting the address and corresponding data to the host computer***...", and Figure 2, "***Status Signal***").

As per claim 2, the rejection of claim 1 is incorporated. Ok discloses the microprocessor system comprises of break point address holders and a break point comparator which receive and compare the break point addresses from the two break point address holder with the address of the user program being executed from the program memory address pointer; (See Figure 3. "52-Address Register" and "53- ***Address Comparator***", Col 6; lines 38-44 "***Executing continuously***"). It is inherent that the Address register of Ok disclosures have the capabilities of holding more than one address because an address register

function as an addresses holder. Further more, it is inherent that the comparator of Ok disclosure can compare more than a set of addresses. If the comparator ran continuously as in Ok disclosures, the comparator can compare more than one set of addresses just using one comparators instead of two.

and the microprocessor system further comprises an interrupt generator for receiving signals of the break point comparators, and outputting a corresponding interrupt control signal to the interrupt control unit (See Fig 2, "***Breakpoint sensing unit***" – Also See Col 3; lines 36-41),.

As per claim 3, the rejection of claim 1 is incorporated. OK discloses a microprocessor system comprising a data memory for storing temporary data generated while executing the program (See Figure 2, "70 – Data memory"; and also Col3, Lines 34-35).

As per claim 4, the rejection of claim 3 is incorporated. Ok discloses a microprocessor system comprises a data memory address pointer for indicating data in the data memory (See Col 3, Lines 42-44 and also See Col 5/6; 67:1-2, "***memory break controller outputs the address and data of the data memory location*** currently accessed by the processor to the host computer.). Where "***memory break controller***" is the "**data address pointer**" claimed.

As per claim 5, the rejection of claim 1 is incorporated. Ok discloses a microprocessor comprises of a data access port for transmitting the break point

address transmitted from the host computer to the break point address holder and for transmitting a control signal to the controller (See Figure 2, "Control Signal (Sending from host to microprocessor)", See Figure 5, "S11", and Col 3; lines 27-28, Figure 3, "52 - Address Register"). From reference Figure 2, Host computer send singal/data to microprocessor, which reside remotely.

As per claim 6, the rejection of claim 1 is incorporated. Ok discloses a microprocessor system where the host computer is a computer device (See Col 3, lines 52-55).

As per claim 8, the rejection of claim 1 is incorporated. Ok discloses that the program memory of the microprocessor system is read/write memory (See Figure 2, "60 – Program Memory"). Figure 2 show the transferring of address to the program memory and retrieval of data from the memory, which is the read/write capabilities of the memory claimed.

Claim 9 is a method claim corresponding to the system of claim 1 and rejected under the same reason as set forth in connection of the rejection of claim 1 and further discloses the executing of a user program (See Col 6; Lines 22-24).

As per claim 10, the rejection of claim 9 is incorporated. Ok discloses the method of claim 9 wherein when receiving the interrupt control signal, a monitor

program is executed to output the status of the user program (See Col 2; Lines 38-40, "***transmitting the address and corresponding data to the host computer***...", and Figure 2, "***Status Signal***").

Claim 11 is a device corresponding to the method of claim 9 and rejected under the same reason as set forth in connection of the rejection of claim 9.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ok, (US Patent No. 6,934,886) hereinafter **Ok**, in view of **Waldie** et al, (US Patent Pub. No. 2002/0065646) hereinafter **Waldie**.

As per claim 7, the rejection of claim 1 is incorporated. Ok discloses a microprocessor system that contain a program memory (See Figure 2, "60 – Program Memory"). Ok did not specifically disclose that the program memory of the microprocessor system is read-only memory. However, Waldie in an analogous art discloses that the program memory can be read only memory (See Waldie; Pages 3, Paragraph [0029] -Lines 6-8). Therefore, it would have been

obvious to a person of ordinary skill in the art at the time of invention was made to incorporate the teaching of Waldie into the system of Ok. The modification would have been obvious because one of the ordinary skill in the art would want to have a permanent memory for storage of data or programs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nha Nguyen whose telephone number is 703-272-1405. The examiner can normally be reached on M-F 7:30 - 5:00 PM EST. (Every other Friday OFF).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nha Nguyen
10/17/2006
A.U 2112

Chameli Das

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SUPERVISORY PATENT EXAMINER

10/23/06